Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1 (Currently Amended). Circuitry for processing images and video, comprising:

a processor for executing software instructions for processing images or video;

a random access memory;

a motion estimation hardware accelerator coupled to said random access memory and the processor for performing motion estimation functions, responsive to a request by the processor, on data from the random access memory and returning a result to the processor for further processing of the video or images in the processor based on the result from the motion estimation hardware accelerator; and

a transform coding hardware accelerator coupled to said random access memory and the processor for performing transform coding functions, responsive to a request by the processor, on data from the random access memory and returning a result to the processor for further processing of the video or images in the processor based on the result from the transform coding hardware accelerator. ~~; and~~

~~a processor coupled to said hardware accelerators and to said random access memory for executing software instructions for processing images and video, wherein some of the instructions initiate functions performed by one or more of said hardware accelerators such that the one or more hardware accelerators retrieve data from the random access memory, perform a function on the data, and return a result to the processor.~~

2 (Original). The circuitry of claim 1 and further comprising a pixel interpolation hardware accelerator coupled to said random access memory.

3 (Original). The circuitry of claim 2 wherein said pixel interpolation hardware accelerator performs a half-pixel interpolation function.

4 (Original). The circuitry of claim 1 wherein said motion estimation hardware accelerator includes circuitry for calculating a mean absolute difference function.

5 (Original). The circuitry of claim 1 wherein said transform coding hardware accelerator includes circuitry for calculating a direct cosine transform function.

6 (Original). The circuitry of claim 5 wherein said transform coding hardware accelerator includes circuitry for calculating an inverse direct cosine transform function.

7 (Currently amended). A method of processing video information, comprising the steps of:

executing a compression task in a programmable processing device coupled to a random access memory;

upon encountering a motion estimation instruction, initiating execution of an associated function in a motion estimation hardware accelerator, said motion estimation hardware accelerator coupled to said processing device and said random access memory, such that the motion estimation hardware accelerator retrieves image data from the random access memory, performs a motion estimation function on the data, and returns a result to the processor for further processing of the compression task in the processor based on the result from the motion estimation hardware accelerator; and

upon encountering a transform coding instruction, initiating execution of an associated function in a transform coding hardware accelerator, said transform coding hardware accelerator coupled to said processing device and said random access memory, such that the transform coding hardware accelerator retrieves image data from the random access memory, performs a transform coding function on the data, and returns a result to the processor for further processing of the compression task in the processor based on the result from the transform coding hardware accelerator.

8 (Previously presented). The method of claim 7 step of initiating execution of an associated function in the motion estimation hardware accelerator includes the step

of retrieving image data from a data portion of said random access memory into said motion estimation hardware accelerator.

9 (Previously presented). The method of claim 7 step of initiating execution of an associated function in the transform coding hardware accelerator includes the step of retrieving image data from a data portion of said random access memory into said transform coding hardware accelerator.

10 (Previously presented). The method of claim 7 and further comprising the step of, upon encountering a pixel interpolation instruction, initiating execution of an associated function in a pixel interpolation hardware accelerator, said pixel interpolation hardware accelerator coupled to said processing device and said random access memory, such that the pixel interpolation hardware accelerator retrieves data from the random access memory, performs an interpolation function on the data, and returns a result to the processor.

11 (Original). The method of claim 10 wherein said step of initiating execution of an associated function in a pixel interpolation hardware accelerator includes the step of performing a half-pixel interpolation function.

12 (Original). The method of claim 7 wherein said step of initiating execution of an associated function in a motion estimation hardware accelerator includes the step of performing a mean absolute difference function.

13 (Original). The method of claim 7 wherein said step of initiating execution of an associated function in a transform coding hardware accelerator includes the step of performing a direct cosine transform function.

14 (Original). The method of claim 13 wherein said step of initiating execution of an associated function in a transform coding hardware accelerator includes the step of performing an inverse direct cosine transform function.

15 (New). Circuitry for processing images and video, comprising:

a processor for executing a program of software instructions for processing images or video;

a random access memory;

a bus for coupling the processor to one or more hardware accelerators for performing certain video processing functions associated with ones of the software instructions;

wherein certain software instructions can be processed by either the processor or a hardware accelerator based on whether a hardware accelerator for processing the certain software instruction is coupled to the bus, where the decision to process the certain software instruction in the processor is made in real-time.